

*In the Claims*

Kindly amend the claims, as follows:

Claims 1-38 (Canceled)

39. (Currently Amended): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive of the node set T with each device in the device set A being capable of sending data to a node in the node set T;

a device set Z mutually exclusive of the node set T with each device in the device set Z being capable of receiving data from a node in the node set T;

a collection C of node sets that are subsets of the node set T, each node in the node set T being contained in exactly one member of the collection C;

for a device x in the device set Z, a sequence  $cx = cx_0, cx_1, cx_2, \dots, cx_U$  exists with each member of the sequence cx being a node set in the collection C, the sequence cx being capable of passing data from devices in the device set A to the device x on a plurality of paths, among the plurality of paths being a path set P(x) characterized in that a path R is included in the path set P(x) only if each node on the path R is in a member of the sequence cx, a node of the path R that receives a message directly from a device in the device set A being in a set having the form  $cx_v$  and a node of the path R that sends data directly to the device x being in a set of the form  $cx_u$  with U being larger than V;

for a member Q of the collection C, a corresponding set of devices Z(Q) exists in the device ~~plurality~~ set Z such that a device q is included in the set of devices Z(Q) only if the member Q is also a member of ~~the~~ a sequence cq;

for members  $CXH$  and  $CXK$  of the sequence  $cx$  with  $H > K$ , a device set  $Z(cx_K)$  is a subset of a device set  $Z(cx_H)$  and a device exists in the device set  $Z(cx_H)$  that is not included in the device set  $Z(cx_K)$ ; and

the node set  $T$  includes three distinct nodes  $p$ ,  $q$ , and  $r$ , the node  $p$  being in a member  $cz_D$  of sequence  $cz$ , the nodes  $q$  and  $r$  being in a member  $cz_E$  of the sequence  $cz$  with  $D > E$ , in one path of paths  $P(x)$  a message moves directly from the node  $p$  to the node  $r$  and in another path of paths  $P(x)$  a message moves directly from the node  $q$  to the node  $r$ .

40. (Currently Amended): An interconnect structure according to Claim 39 wherein:

the paths  $P(x)$  include a path such that if a message hops from a node in a member  $cz_n$  to a node in a member  $cz_m$ , then  $n \geq m$ .

41. (Previously presented): An interconnect structure according to Claim 39 wherein:

the collection  $C$  includes distinct member node sets  $D$  and  $E$ , and for corresponding device sets  $Z(D)$  and  $Z(E)$  with the device set  $Z(D)$  being a subset of the device set  $Z(E)$ , a device  $y$  in the device set  $Z(D)$  exists such that member node set  $D$  is a node set  $cy_R$  and member node set  $E$  is a node set  $cys$  and  $R$  is greater than  $S$ .

42. (Currently Amended): An interconnect structure according to Claim 39 further comprising:

an arrangement of the nodes in the interconnect structure into a hierarchy of levels of node sets  $L = L_0, L_1, \dots, L_J$ , each member of the hierarchy  $L$  being a node set that is subset of the node set  $T$  and each node in the node set  $T$  is contained in exactly one member of the node sets  $L$ ; and

for the device  $x$  of the device set  $Z$ , a node set  $cx_N$  is a subset of the a level  $N$  node set  $L_N$ , with  $N$  not exceeding  $J$ .

43. (Previously presented): An interconnect structure according to claim 42 wherein:

a message  $M_y$  targeted for a device  $y$  in the device set  $Z$  enters at a node on level  $L_j$  and exits at an output port on level  $L_0$  with the output port being connected to the device  $y$ ; and

for a hop in a path of the message  $M_y$  from a node of  $L_U$  to a node of  $L_V$ ,  $U$  being greater than or equal to  $V$ .

44. (Currently Amended): An interconnect structure according to claim 43 wherein:

the collection  $C$  includes  $2^{J-N}$  members on a level  $N$ ;

the collection  $C$  includes three members  $D$ ,  $E$  and  $F$  such that member node set  $D$  is on the level  $L_N$  and member node sets  $E$  and  $F$  are on the a level  $L_{N-1}$ ;

the interconnect set  $I$  includes interconnects positioned to allow data to pass directly from the member node set  $D$  to the member node set  $E$  and to pass directly from the node set  $D$  to the node set  $F$ ; and

the device set  $Z$  includes device sets  $Z(D)$ ,  $Z(E)$ , and  $Z(F)$  that correspond to the three members  $D$ ,  $E$ , and  $F$ , the device sets  $Z(E)$  and  $Z(F)$  being mutually exclusive device sets, and the device set  $Z(D)$  is the union of the device sets  $Z(E)$  and  $Z(F)$ .

45. (Previously presented): An interconnect structure according to Claim 39 further comprising:

a member node set  $c$  in the collection  $C$ ; and

a plurality of interconnects in the interconnect set  $I$  connecting nodes in the member  $c$  so that the nodes of the node set  $c$  are arranged in a ring.

46. (Currently Amended): An interconnect structure in accordance with Claim 39 further comprising:

a logic  $L_p$  associated with the node  $p$  wherein for a message  $M_p$  that arrives at the node  $p$ , the logic  $L_p$  uses information concerning the sending of messages

from the node q for the logic Lp to determine where the node ~~p~~ p is to send the message Mp.

47. (Previously Presented): An interconnect structure according to claim 46 wherein:

the node q has priority over the node p to send data to the node r so that a message Mq located at the node q is not blocked from being sent to the node r by a message Mp at the node p.

48. (Previously Presented): An interconnect structure according to claim 47 wherein:

the node q is capable of sending a control signal to the node p wherein the purpose of the control signal is to enforce the priority of the node q over the node p to send data to the node r.

49. (Previously Presented): An interconnect structure according to Claim 39 wherein:

the node set T is a proper subset of nodes in the interconnect structure; and the interconnect set I is a proper subset of the interconnects in the interconnect structure.

50. (Previously Presented): An interconnect structure according to Claim 39 wherein:

each node in the interconnect structure is included in the node set T; and each interconnect in the interconnect structure is included in the interconnect set I.

51. (Currently Amended): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive of the node set T with each device in the device set A being capable of sending data to a node in the node set T;

a device set Z mutually exclusive of the node set T with each device in the device set Z being capable of receiving data from a node in the node set T;

a collection C of node sets that are subsets of the node set T, each node in the node set T being contained in exactly one member of the collection C;

for a device x in the device set Z, a sequence  $cx = cx_0, cx_1, cx_2, \dots, cx_j$  exists with each member of the sequence cx being a node set in the collection C, the sequence cx being capable of passing data from devices in the device set A to the device x on a plurality of paths, among the plurality of paths being a path set  $P(x)$  characterized in that a path R is included in the path set  $P(x)$  only if each node on the path R is in a member of the sequence cx, a node of the path R that receives a message directly from a device in the device set A being in a set having the form  $cx_U$  and a node of the path R that sends data directly to the device x being in a set of the form  $cx_V$  with U being larger than V;

for a member Q of the collection C, a corresponding set of devices  $Z(Q)$  exists in the device ~~plurality~~ set Z such that a device q is included in the set of devices  $Z(Q)$  only if the member Q is also a member of the a sequence  $cq$ ;

for members  $cx_H$  and  $cx_K$  of the sequence cx with  $H > K$ , a device set  $Z(cx_K)$  is a subset of a device set  $Z(cx_H)$  and a device exists in the device set  $Z(cx_H)$  that is not included in the device set  $Z(cx_K)$ ; and

the node set T includes three distinct nodes p, q, and r, the nodes p and q being in a member  $cz_D$  of sequence cz, the node r being in a member  $cz_E$  of the sequence cz with  $D > E$ , in a first path of paths  $P(x)$  a message moves directly from the node p to the node q, in a second path of paths  $P(x)$  a message moves directly from the node p to the node r.

52. (Currently Amended): An interconnect structure according to Claim 51 wherein:

the paths  $P(x)$  include a path such that if a message hops from a node in a member  $cz_n$  to a node in a member  $cz_m$ , then  $n \geq m$ .

53. (Currently Amended): An interconnect structure according to Claim 51 further comprising:

an arrangement of the nodes in the interconnect structure into a hierarchy of levels of node sets  $L = L_0, L_1, \dots, L_J$  each member of the hierarchy  $L$  being a node set that is subset of the node set  $T$  and each node in the node set  $T$  is contained in exactly one member of the node set  $L$ ; and

for the device  $x$  of the device set  $Z$ , member node set  $cz_N$  is a subset of ~~the~~ a level  $N$  node set  $L_N$ ,  $N$  not exceeding  $J$ .

54. (Previously Presented): An interconnect structure according to Claim 53 wherein:

a message  $M_y$  targeted for a device  $y$  in the device set  $Z$  enters at a node on level  $L_J$  and exits at an output port on level  $L_0$  with the output port being connected to the device  $y$ ; and

for a hop in a path of the message  $M_y$  from a node of  $L_U$  to a node of  $L_V$ ,  $U$  being greater than or equal to  $V$ .

55. (Currently Amended): An interconnect structure according to Claim 54 wherein:

the collection  $C$  includes  $2^{J-N}$  members on a level  $N$ ;

the collection  $C$  includes three members  $D$ ,  $E$  and  $F$  such that member node set  $D$  is on the level  $L_N$  and member node sets  $E$  and  $F$  are on ~~the~~ a level  $L_{N-1}$ ;

the interconnect set  $I$  includes interconnects positioned to allow data to pass directly from the member node set  $D$  to the member node set  $E$  and to pass directly from the node set  $D$  to the node set  $F$ ; and

the device set  $Z$  includes device sets  $Z(D)$ ,  $Z(E)$ , and  $Z(F)$  that correspond to the three members  $D$ ,  $E$ , and  $F$ , the device sets  $Z(E)$  and  $Z(F)$  being mutually exclusive device sets, and the device set  $Z(D)$  is the union of the device sets  $Z(E)$  and  $Z(F)$ .

56. (Previously Presented): An interconnect structure according to Claim 51 further comprising:

a member node set  $c$  in the collection  $C$ ; and

a plurality of interconnects in the interconnect set  $I$  connecting nodes in the member  $c$  so that the nodes of the node set  $c$  are arranged in a ring.

57. (Currently Amended): An interconnect structure comprising:

a plurality of nodes including a node  $N_E$  and a node set  $P$ , the node set  $P$  including a plurality of nodes that are capable of sending data to the node  $N_E$ ; and

a plurality of interconnect paths interconnecting the plurality of nodes, the interconnect paths including data interconnect paths that couple nodes in pairs, a node pair including a sending node and a receiving node, the sending node being capable of sending data to the receiving node;

the nodes in the node set  $P$  having a priority relationship for sending data to the node  $N_E$ , the nodes ~~in~~ in the node set  $P$  including distinct nodes  $N_F$  and  $N_A$ , the node  ~~$N_F$~~   $N_F$  having a highest priority among the nodes in the node set  $P$  for sending data to the node  $N_E$  so that ~~the~~ a message  $M_F$  arriving at the node  $N_F$  is not blocked from traveling to the node  $N_E$  by ~~the~~ a message  $M_A$  arriving at the node  $N_A$ ; and

for a message  $M$  arriving at the node  $N_A$  and the message  $M$  is blocked from being sent to the node  $N_E$ , then the blocking of the message  $M$  from being sent to the node  $N_E$  causes , sending of the message  $M$  from the node  $N_A$  to a node distinct from the node  $N_E$ .

58. (Currently Amended): An interconnect structure according to Claim 57 wherein:

the node  $N_F$  is capable of sending data to a node  $N_T$  distinct from the nodes  $N_F$  and  $N_E$ .

59. (Previously Presented): An interconnect structure according to Claim 57 wherein:

a node  $N_U$  of the node set  $p$  is not blocked from sending data to the node  $N_E$  as a result of data sent to the node  $N_E$  from a node  $N_V$  having a priority lower than the node  $N_U$  for sending data to the node  $N_E$ .

60. (Currently Amended): An interconnect structure according to Claim 57 wherein:

the priority relationship among the nodes in the node set  $P$  capable of sending data to the node  $N_E$  depends on the position of the individual nodes in the node set  $P$  within the interconnect structure.

61. (Previously Presented): An interconnect structure according to Claim 57 further comprising:

the plurality of nodes including the distinct nodes  $N_A$ ,  $N_E$ , and  $N_F$ ; a plurality of logic elements associated with the plurality of nodes;

a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling the plurality of nodes in pairs including a receiving node and a sending node capable of sending data to the receiving node;

a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with the sending node to a logic element associated with the receiving node;

the plurality of nodes including:

a logic  $L_A$  associated with the node  $N_A$  that makes routing decisions for the node  $N_A$ ;

a data interconnect path from the node  $N_F$  operative as the sending node to the node  $N_E$  operative as the receiving node;

a data interconnect path from the node  $N_A$  operative as the sending node to the node  $N_E$  operative as the receiving node; and

a control signal interconnect path from a source associated with the node  $N_F$  operative as a sending node to the logic  $L_A$ , the control signal



enforcing a priority for sending data from the node  $N_F$  to the node  $N_E$  over sending data from the node  $N_A$  to the node  $N_E$ .

62. (Currently Amended): An interconnect structure according to Claim 57 further comprising:

the plurality of nodes including the node  $N_F$ , the node  $N_A$ , and a node set  $R$ , the nodes  $N_F$  and  $N_A$  being distinct nodes that are excluded from the node set  $R$ , the node  $N_A$  being capable of sending data to each node in the node set  $R$ ;

the plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

the a plurality of control interconnect paths coupling the plurality of nodes, a the control interconnect ~~path~~ paths used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node  $N_F$  to ~~the~~ a logic  $L_A$  associated with the node  $N_A$ , the logic  $L_A$  using a control signal from a source associated with the node  $N_F$  to determine to which node of the node set  $R$  the node  $N_A$  sends data.

63. (Currently Amended): An interconnect structure according to Claim 57 wherein:

the plurality of nodes include the nodes  $N_A$ ,  ~~$N_D$~~ ,  $N_E$ , and  $N_F$ , and a node  $N_D$ ;

the interconnect paths include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control- signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;

the plurality of interconnect paths further include data interconnect paths for sending data from the node  $N_A$  to the node  $N_E$  and to the node  $N_D$ , and a control interconnect path for sending a control signal from a source associated with the node  $N_F$  to ~~the~~ a logic element  $L_A$  associated with the node  $N_A$ , and

for a message M arriving at the node  $N_F$ , a source associated with the node  $N_F$  sends a control signal S to the logic element  $L_A$ , the logic element  $L_A$  using the control signal S to determine between sending the message M to the node  $N_E$  or to the node  $N_D$ .

64. (Currently Amended): An interconnect structure according to Claim 57 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including distinct nodes  $N_F$ ,  $N_A$ ,  $N_E$ , and  $N_D$ ;

the plurality of data-carrying interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

the a plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element  $L_A$  associated with the node  $N_A$ , the logical element  $L_A$  that uses a control signal from a source associated with the node  $N_F$  to determine where to route a message M passing through the node  $N_A$ , a control signal S received from a source associated with the node  $N_F$  that causes sending of the message M from the node  $N_A$  to the node  $N_E$ , and a control signal S' received from the node  $N_F$  that causes sending of the message M from the node  $N_A$  to the node  $N_D$ .

65. (Previously Presented): An interconnect structure according to Claim 57 further comprising:

one or more output ports in which each output port that is accessible from the node  $N_F$  is also accessible from the node  $N_E$ .

66. (Previously Presented): An interconnect structure according to Claim 57 further comprising:

one or more output ports in which an output port that is accessible from the node  $N_A$  is not accessible from the node  $N_E$ .

67. (Currently Amended): An interconnect structure according to Claim 57 further comprising:

the distinct nodes  $N_A$  and  $N_F$  of the plurality of nodes;

means for sending a plurality of messages including a the message  $M_A$  and a the message  $M_F$  through the interconnect structure nodes, the message  $M_F$  including one or more header bits;

means for routing the message  $M_F$  to enter the node  $N_F$  of the interconnect structure;

means for routing the message  $M_A$  to enter the node  $N_A$  of the interconnect structure;  
and

means for using header bits of the message  $M_F$  at the node  $N_F$  to route the message  $M_A$  from the node  $N_A$ .

68. (Currently Amended): An interconnect structure comprising:

a plurality of nodes including a node  $N_E$  and a node set  $P$ , the node set  $P$  including a plurality of nodes that are capable of sending data to the node  $N_E$ ; and

a plurality of interconnect paths interconnecting the plurality of nodes, the interconnect paths including data interconnect paths that couple nodes in pairs including a receiving node and a sending node that is capable of sending data to the receiving node; and

the nodes in the node set  $P$  having a priority relationship for sending data to the node  $N_E$ , the nodes in the node set  $P$  including distinct nodes  $N_F$  and  $N_A$ , the node  $N_F$  having a highest priority among the nodes in the node set  $P$  for sending data to the node  $N_E$ , ~~the a~~ message  $M_F$  arriving at the node  $N_F$  is not blocked from traveling to the node  $N_E$  by ~~the a~~ message  $M_A$  arriving at the node  $N_A$ , wherein:

when a message  $M$  arrives at the node  $N_A$  and is targeted for the node  $N_E$  and not blocked by a message  $M'$  arriving at a node in the node set  $P$  having a higher priority than the node  $N_A$  for sending messages to the node  $N_F$ , the node  $N_A$  sends the message  $M$  to the node  $N_E$ .

69. (Currently Amended): An interconnect structure according to Claim 68 wherein:

the node  $N_F$  is capable of sending data to a node  $N_T$  distinct from the nodes  $N_F$  and  $N_E$ .

70. (Previously Presented): An interconnect structure according to Claim 68 wherein:

a node  $N_U$  of the node set  $P$  is not blocked from sending data to the node  $N_E$  as a result of data sent to the node  $N_E$  from a node  $N_V$  having a priority lower than the node  $N_U$  for sending data to the node  $N_E$ .

71. (Previously Presented) An interconnect structure according to Claim 68 wherein:

the priority relationship among the nodes in the node set  $P$  capable of sending data to the node  $N_E$  depends on the position of the individual nodes in the node set  $P$  within the interconnect structure.

72. (Previously Presented): An interconnect structure according to Claim 68 further comprising:

the plurality of nodes including the distinct nodes  $N_A$ ,  $N_E$ , and  $N_F$ ;

a plurality of logic elements associated with the plurality of nodes;

a plurality of data interconnect paths coupling the plurality of nodes, a data

interconnect path coupling the plurality of nodes in pairs including a receiving node and a sending node capable of sending data to the receiving node;

a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with the sending node to a logic element associated with the receiving node;

a logic  $L_A$  associated with the node  $N_A$  that makes routing decisions for the node  $N_A$ ;

a data interconnect path from the node  $N_F$  operative as the sending node to the node  $N_E$  operative as the receiving node;

a data interconnect path from the node  $N_A$  operative as the sending node to the node  $N_E$  operative as the receiving node; and

a control signal interconnect path from a source associated with the node  $N_F$  operative as a sending node to the logic  $L_A$ , the control signal enforcing a priority for sending data from the node  $N_F$  to the node  $N_E$  over sending data from the node  $N_A$  to the node  $N_E$ .

73. (Currently Amended): An interconnect structure according to Claim 68 further comprising:

the plurality of nodes including the node  $N_F$ , the node  $N_A$ , and a node set  $R$ , the nodes  $N_F$  and  $N_A$  being distinct nodes that are excluded from the node set  $R$ , the node  $N_A$  being capable of sending data to each node in the node set  $R$ ;

the plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

~~the~~ a plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node  $N_F$  to ~~the~~ a logic  $L_A$  associated with the node  $N_A$ , the logic  $L_A$  using a control signal from a source associated with the node  $N_F$  to determine to which node of the node set  $P$  the node  $N_A$  sends data.

74. (Currently Amended): An interconnect structure according to Claim 68 wherein:

the plurality of nodes include the nodes  $N_A$ ,  $N_D$ ,  $N_E$ , and  $N_F$ , ~~and a node  $N_D$~~ ;

the interconnect paths include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control-signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;

the plurality of interconnect paths further include data interconnect paths for sending data from the node  $N_A$  to the node  $N_E$  and to the node  $N_D$ , and a control

interconnect path for sending a control signal from a source associated with the node  $N_F$  to ~~the~~ a logic element  $L_A$  associated with the node  $N_A$ , and for a message  $M$  arriving at the node  $N_F$ , a source associated with the node  $N_F$  sends a control signal  $S$  to the logic element  $L_A$ , the logic element  $L_A$  using the control signal  $S$  to determine between sending the message  $M$  to the node  $N_F$  or to the node  $N_D$ .

75. (Currently Amended): An interconnect structure according to Claim 68 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including distinct nodes  $N_F$ ,  $N_A$ ,  $N_E$ , and  $N_D$ ;

the plurality of ~~data-carrying data~~ interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

~~the~~ a plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element  $L_A$  associated with the node  $N_A$ , the logical element  $L_A$  that uses a control signal from a source associated with the node  $N_F$  to determine where to route a message  $M$  passing through the node  $N_A$ , a control signal  $S$  received from a source associated with the node  $N_F$  that causes sending of the message  $M$  from the node  $N_A$  to the node  $N_E$ , and a control signal  $S'$  received from the node  $N_F$  that causes sending of the message  $M$  from the node  $N_A$  to the node  $N_D$ .

76. (Currently Amended): An interconnect structure according to Claim 68 further comprising:

one or more output ports in which each output port that is accessible from the node  $N_F$  is also ~~1~~ accessible from the node  $N_E$ .

77. (Previously Presented): An interconnect structure according to Claim 68 further comprising:

one or more output ports in which an output port that is accessible from the node  $N_A$  is not accessible from the node  $N_E$ .

78. (Currently Amended): An interconnect structure according to Claim 68 further comprising:

the distinct nodes  $N_A$  and  $N_F$  of the plurality of nodes;

means for sending a plurality of messages including a message  $M_A$  and a message  $M_F$  through the interconnect structure nodes, the message  $M_F$  including one or more header bits;

means for routing the message  $M_F$  to enter the node  $N_F$  of the interconnect structure;

means for routing the message  $M_A$  to enter the node  $N_A$  of the interconnect structure;  
and

means for using header bits of the message  $M_F$  at the node  $N_F$  to route the message  $M_A$  from the node  $N_A$ .

79. (Currently Amended): An interconnect structure  $S$  containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

a node set  $T$ ;

an interconnect set  $I$  that selectively connects nodes in the node set  $T$ ;

a device set  $A$  mutually exclusive with the node set  $T$  with each device in the device set  $A$  capable of sending data to a node in the node set  $T$ ;

a device set  $Z$  mutually exclusive with the node set  $T$  with each device in the device set  $Z$  capable of receiving data from a node in the node set  $T$ ;

a set of data-carrying paths  $P$ , each path of the path set  $P$  being capable of carrying data from a device in the device set  $A$  to a device in the device set  $Z$ , each node on the path of the path set  $P$  is included in the node set  $T$ , and each interconnect in the path is included in the interconnect set  $I$ ;

a node set  $U$  characterized as the set of nodes within the node set  $T$  that are on a path included in the path set  $P$ ;

for a node  $N$  in the node set  $T$  such that the node  $N$  is on a path in the path set  $P$ , a corresponding set of devices  $Z(N)$  exists in the device set  $Z$  such that a device  $w$  is, included in the device set  $Z(N)$  only if a path exists in the path set  $P$  from a member of the device set  $A$  to the device  $w$  such that the path contains the node  $N$ ; and

the node set  $U$  includes three distinct nodes  $N_A$ ,  $N_D$ , and  $N_E$  such that the node  $N_A$  is capable of sending data to the node  $N_D$  and the node  $N_E$ , and a device set  $Z(N_A)$  is the same as a device set  $Z(N_D)$ , and a device set  $Z(N_E)$  is a proper subset of the device set  $Z(N_A)$ .

80. (Previously Presented): An interconnect structure according to Claim 79 wherein:

the interconnect  $S$  is a part of a larger interconnect structure  $T$ .

81. (Previously Presented): An interconnect structure according to Claim 79 further comprising:

the interconnect  $S$  is not a subset of a larger interconnect structure  $T$ .

82. (Previously Presented): An interconnect structure according to Claim 79 wherein:

a time  $T_A$  is associated with the node  $N_A$  such that messages arriving at the node  $N_A$  are sent to another node within the time  $T_A$  of the messages' arrival at the node  $N_A$ .

83. (Previously Presented): An interconnect structure according to Claim 79 further comprising:

a logic element  $L_A$  associated with the node  $N_A$  that determines routing from the node  $N_A$ ;

a node  $N_X$  distinct from the node  $N_A$ ;

a logical element  $L_X$  associated with the node  $N_X$  that determines routing for the node  $N_X$ , the logical element  $L_X$  being distinct from the logical element  $L_A$ .



84. (Previously Presented): An interconnect structure according to Claim 79 further comprising:

the plurality of nodes including a node  $N_F$ , the nodes  $N_A$ ,  $N_E$ , and  $N_F$  being mutually distinct;

a plurality of logic elements associated with the plurality of nodes;

a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling the plurality of nodes in pairs including a receiving node and a sending node capable of sending data to the receiving node;

a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with the sending node to a logic element associated with the receiving node;

the plurality of nodes including:

a logic  $L_A$  associated with the node  $N_A$  that makes routing decisions for the node  $N_A$ ;

a data interconnect path from the node  $N_F$  operative as the sending node to the node  $N_E$  operative as the receiving node;

a data interconnect path from the node  $N_A$  operative as the sending node to the node  $N_E$  operative as the receiving node; and

a control signal interconnect path from a source associated with the node  $N_F$  operative as a sending node to the logic  $L_A$ , the control signal enforcing a priority for sending data from the node  $N_F$  to the node  $N_E$  over sending data from the node  $N_A$  to the node  $N_E$ .

85. (Currently Amended): An interconnect structure according to Claim 79 further comprising:

the plurality of nodes including a node  $N_F$  and a node set  $R$ , the nodes  $N_F$  and  $N_A$  being distinct nodes that are excluded from the node set  $R$ , the node  $N_A$  being capable of sending data to each node in the node set  $R$ ;

the a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and

the a plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, the plurality of control interconnect paths including a control interconnect path from a source associated with the node  $N_F$  to the a logic  $L_A$  associated with the node  $N_A$ , the logic  $L_A$  using a control signal from a source associated with the node  $N_F$  to determine to which node of the node set  $R$  the node  $N_A$  sends data.

86. (Previously Presented): An interconnect structure according to Claim 85 wherein:

the node  $N_A$  is capable of sending data only to nodes in the node set  $R$ .

87. (Previously Presented): An interconnect structure according to Claim 85 wherein:

the node  $N_A$  is capable of sending data to a node outside the node set  $R$ .

88. (Currently Amended): An interconnect structure according to Claim 79 wherein further comprising:

the plurality of nodes include including a node  $N_F$ ;

the a plurality of interconnect paths include including control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control-signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node; the plurality of interconnect paths further include including data interconnect paths for sending data from the node  $N_A$  to the node  $N_E$  and to the node  $N_D$ , and a control interconnect path for sending a control signal from a source associated with the node  $N_F$  to the a logic element  $L_A$  associated with the node  $N_A$ , and for a message  $M$  arriving at the node  $N_F$ , a source associated with the node  $N_F$  sends a control signal  $S$  to the logic element  $L_A$ , the logic element  $L_A$  using the control

signal S to determine between sending the message M to the node  $N_E$  or to the node  $N_D$ .

89. (Previously Presented): An interconnect structure according to Claim 88 wherein:

a message  $M'$  arriving at the node  $N_A$  is routed to a node  $N_Z$  distinct from the nodes  $N_E$ ,  $N_D$ , and  $N_F$ ,

90. (Previously Presented): An interconnect structure according to Claim 88 wherein:

the control interconnect path from the node  $N_F$  to the node  $N_A$  is a direct link from a logic  $L_F$  associated with the node  $N_F$  to the logic  $L_A$ .

91. (Previously Presented): An interconnect structure according to Claim 88 wherein:

the control signal sent to the node  $N_A$  is tapped from an output data port of the node  $N_F$ .

92. (Currently Amended): An interconnect structure according to Claim 79 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including a node  $N_F$ , the nodes  $N_F$ ,  $N_A$ ,  $N_E$ , and  $N_D$  being mutually distinct;

the ~~plurality set~~ of data-carrying ~~interconnect~~ paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

~~the~~ a plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element  $L_A$  associated with the node  $N_A$ , the logical element  $L_A$  that uses a control signal from a source associated with the node  $N_F$  to determine where to route a message M passing through the node  $N_A$ , a control signal S received

from a source associated with the node  $N_F$  that causes sending of the message  $M$  from the node  $N_A$  to the node  $N_E$ , and a control signal  $S'$  received from the node  $N_F$  that causes sending of the message  $M$  from the node  $N_A$  to the node  $N_D$ .

93. (Previously Presented): An interconnect structure according to Claim 92 wherein:

the control signal interconnection path is a direct link from the node  $N_F$  to the node  $N_A$ .

94. (Previously Presented): An interconnect structure according to Claim 92 wherein:

routing of a message  $M'$  passing through the node  $N_A$  is the same whether the control signal from the node  $N_F$  is the control signal  $S$  or the control signal  $S'$ .

95. (Previously Presented): An interconnect structure according to Claim 92 wherein:

the control signal sent to the logic  $L_A$  is tapped from an output data port of the node  $N_F$ .

96. (Previously Presented): An interconnect structure according to Claim 79 further comprising:

distinct nodes  $N_A$  and  $N_F$  of the plurality of nodes;

means for sending a plurality of messages including a message  $M_A$  and a message  $M_F$  through the interconnect structure nodes, the message  $M_F$  including one or more header bits;

means for routing the message  $M_F$  to enter the node  $N_F$  of the interconnect structure;

means for routing the message  $M_A$  to enter the node  $N_A$  of the interconnect structure;  
and

means for using header bits of the message  $M_F$  at the node  $N_F$  to route the message  $M_A$  from the node  $N_A$ .

97. (Previously Presented): An interconnect structure according to Claim 96 wherein:

the means for routing the message  $M_F$  uses the one or more header bits of the message  $M_F$  to route the message  $M_F$ ; and  
the means for routing the message  $M_A$  uses information relating to the routing of the message  $M_F$  to route the message  $M_A$ .

98. (Currently Amended): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure comprising:

- a node set T;
- an interconnect set I that selectively connects nodes in the node set T;
- a device set A mutually exclusive with the node set T with each device in the device set A capable of sending data to a node in the node set T;
- a device set Z mutually exclusive with the node set T with each device in the device set Z capable of receiving data from a node in the node set T;
- a set of data-carrying paths P, each path being capable of carrying data from a device in the device set A to a device in the device set Z, each node on the path is included in the node set T, and each interconnect in the path is included in the interconnect set I;
- a node set U characterized as the set of nodes within the node set T that are on a path included in the path set P;
- for an interconnect link L in the interconnect set I, the interconnect link L being an interconnect link on a path in the path set P, a corresponding set of devices Z(L) exists in the device set Z such that a device w is included in the device set Z(L) only if a path containing the interconnect link L in the path set P exists from a device in the device set A to the device w; and
- the node set U includes distinct nodes  $N_A$ ,  $N_D$ , and  $N_E$  such that the node  $N_A$  is capable of sending data to the node  $N_D$  on a link  $L_{AD}$ , the node  $N_A$  is capable of sending data to the node  $N_E$  on a link  $L_{AE}$ , and the a device set  $Z(L_{AE})$  is a proper subset of the a device subset  $Z(L_{AD})$ .

99. (Previously Presented): An interconnect structure according to Claim 98 wherein:

the interconnect S is a part of a larger interconnect structure T.

100. (Previously Presented): An interconnect structure according to Claim 98 further comprising:

the interconnect S is not a subset of a larger interconnect structure T.

101. (Previously Presented): An interconnect structure according to Claim 98 wherein:

a time  $T_A$  is associated with the node  $N_A$  such that messages arriving at the node  $N_A$  are sent to another node within the time  $T_A$  of the messages' arrival at the node  $N_A$ .

102. (Previously Presented): An interconnect structure according to Claim 98 further comprising:

a logic element  $L_A$  associated with the node  $N_A$  that determines routing from the node  $N_A$ ;

a node  $N_X$  distinct from the node  $N_A$ ;

a logical element  $L_X$  associated with the node  $N_X$  that determines routing for the node  $N_X$ , the logical element  $L_X$  being distinct from the logical element  $L_A$ .

103. (Previously Presented): An interconnect structure according to Claim 98 further comprising:

the plurality of nodes including a node  $N_F$ , the nodes  $N_A$ ,  $N_E$ , and  $N_F$  being mutually distinct;

plurality of logic elements associated with the plurality of nodes;

a plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling the plurality of nodes in pairs including a receiving node and a sending node capable of sending data to the receiving node;

a plurality of control signal interconnect paths coupling the plurality of nodes to send a control signal from a source associated with the sending node to a logic element associated with the receiving node;

the plurality of nodes including:

- a logic  $L_A$  associated with the node  $N_A$  that makes routing decisions for the node  $N_A$ ;
- data interconnect path from the node  $N_F$  operative as the sending node to the node  $N_E$  operative as the receiving node;
- a data interconnect path from the node  $N_A$  operative as the sending node to the node  $N_E$  operative as the receiving node; and
- a control signal interconnect path from a source associated with the node  $N_F$  operative as a sending node to the logic  $L_A$ , the control signal enforcing a priority for sending data from the node  $N_F$  to the node  $N_E$  over sending data from the node  $N_A$  to the node  $N_E$ .

104. (Currently Amended): An interconnect structure according to Claim 98 further comprising:

- the plurality of nodes including a node  $N_F$  and a node set  $R$ , the nodes  $N_F$  and  $N_A$  being distinct nodes that are excluded from the node set  $R$ , the node  $N_A$  being capable of sending data to each node in the node set  $R$ ;
- ~~the a~~ plurality of data interconnect paths coupling the plurality of nodes, a data interconnect path coupling a pair of the plurality of nodes as a sending node capable of sending data to a receiving node; and
- ~~the a~~ plurality of control interconnect paths coupling the plurality of nodes, a control interconnect path used to carry control signals from a source associated with a control signal sending node to a logic associated with a control signal using node, and
- the plurality of control interconnect paths including a control interconnect path from a source associated with the node  $N_F$  to the logic  $L_A$  associated with the node  $N_A$ , the logic  $L_A$  using a control signal from a source associated with the node  $N_F$  to determine to which node of the node set  $R$  the node  $N_A$  sends data.

105. (Previously Presented): An interconnect structure according to Claim 104 wherein:

- the node  $N_A$  is capable of sending data only to nodes in the node set  $R$ .

106. (Previously Presented): An interconnect structure according to Claim 104 wherein:

the node  $N_A$  is capable of sending data to a node outside the node set R.

107. (Currently Amended): An interconnect structure according to Claim 98 wherein:

the plurality of nodes include a node  $N_F$ ;

the ~~interconnect paths~~ plurality of interconnects include control interconnect paths and data interconnect paths, the control interconnect paths capable of sending a control signal from a source associated with a control-signal-sending node to a logic associated with a control-signal-using node, the data interconnect paths capable of sending data from a data sending node to a data receiving node;

the plurality of ~~interconnect paths~~ plurality of interconnects further include data interconnect paths for sending data from the node  $N_A$  to the node  $N_E$  and to the node  $N_D$ , and a control interconnect path for sending a control signal from a source associated with the node  $N_F$  to ~~the~~ a logic element  $L_A$  associated with the node  $N_A$  and

for a message M arriving at the node  $N_F$ , a source associated with the node  $N_F$  sends a control signal S to the logic element  $L_A$ , the logic element  $L_A$  using the control signal S to determine between sending the message M to the node  $N_E$  or to the node  $N_D$ .

108. (Previously Presented): An interconnect structure according to Claim 107 wherein:

a message M' arriving at the node  $N_A$  is routed to a node  $N_Z$  distinct from the nodes  $N_E$ ,  $N_D$ , and  $N_F$ .

109. (Previously Presented): An interconnect structure according to Claim 107 wherein:

the control interconnect path from the node  $N_F$  to the node  $N_A$  is a direct link from a logic  $L_F$  associated with the node  $N_F$  to the logic  $L_A$ .



110. (Previously Presented): An interconnect structure according to Claim 107 wherein:

the control signal sent to the node  $N_A$  is tapped from an output data port of the node  $N_F$ .

111. (Currently Amended): An interconnect structure according to Claim 98 further comprising:

the plurality of nodes including input data ports, output data ports, and a plurality of logical elements that control the flow of data through the nodes, the plurality of nodes including a node  $N_F$ , the nodes  $N_F$ ,  $N_A$ ,  $N_E$ , and  $N_D$  being mutually distinct;

~~the a~~ a plurality of data-carrying interconnect paths coupling the plurality of nodes to form paths from the output data ports of data sending nodes to the input data ports of data receiving nodes;

~~the a~~ a plurality of control signal interconnect paths for sending control signals to a logical element associated with a node having a data flow that depends on the control signals; and

a logical element  $L_A$  associated with the node  $N_A$ , the logical element  $L_A$  that uses a control signal from a source associated with the node  $N_F$  to determine where to route a message  $M$  passing through the node  $N_A$ , a control signal  $S$  received from a source associated with the node  $N_F$  that causes sending of the message  $M$  from the node  $N_A$  to the node  $N_E$ , and a control signal  $S'$  received from the node  $N_F$  that causes sending of the message  $M$  from the node  $N_A$  to the node  $N_D$ .

112. (Previously Presented): An interconnect structure according to Claim 111 wherein:

the control signal interconnection path is a direct link from the node  $N_F$  to the node  $N_A$ .

113. (Previously Presented): An interconnect structure according to Claim 111 wherein:

routing of a message  $M'$  passing through the node  $N_A$  is the same whether the control signal from the node  $N_F$  is the control signal  $S$  or the control signal  $S'$

114. (Previously Presented): An interconnect structure according to Claim 111 wherein:

the control signal sent to the logic  $L_A$  is tapped from an output data port of the node  $N_F$ .

115. (Previously Presented): An interconnect structure according to Claim 98 further comprising:

distinct nodes  $N_A$  and  $N_F$  of the plurality of nodes;

means for sending a plurality of messages including a message  $M_A$  and a message  $M_F$  through the interconnect structure nodes, the message  $M_F$  including one or more header bits;

means for routing the message  $M_F$  to enter the node  $N_F$  of the interconnect structure;

means for routing the message  $M_A$  to enter the node  $N_A$  of the interconnect structure; and

means for using header bits of the message  $M_F$  at the node  $N_F$  to route the message  $M_A$  from the node  $N_A$ .30.

116. (Previously Presented): An interconnect structure according to Claim 115 wherein:

the means for routing the message  $M_F$  uses the one or more header bits of the message  $M_F$  to route the message  $M_F$ ; and

the means for routing the message  $M_A$  uses information relating to the routing of the message  $M_F$  to route the message  $M_A$ .